CLAIMS

What is claimed is:

1. A SONET multiplexed communications system, comprising:

at least one SONET input signal path configured to receive at least one input signal;

at least one SONET output signal path configured to transmit at least one output signal corresponding to the input signal; and

a time slot interchange circuit operatively coupled between the SONET input and output signal paths and configured to provide time division multiplexed connections for the input and output signals,

wherein the SONET input signal path includes a pointer interpreter configured to interpret at least one input signal pointer serially coupled to a synchronization buffer configured to transfer the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit, and

wherein the SONET output signal path includes a pointer generator configured to generate at least one output signal pointer serially coupled to a first-in first-out buffer configured to transfer the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path.

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2. The system of claim 1 wherein the pointer interpreter precedes the synchronization buffer in the SONET input signal path.

3. The system of claim 1 wherein the synchronization buffer precedes the pointer interpreter in the SONET input signal path.

4. The system of claim 1 wherein the input signal is an STS-M (M > 1) signal, and the SONET input signal path further includes an alignment buffer operatively coupled between the synchronization buffer and the time slot interchange circuit and configured to perform column alignment on the STS-M signal.

5. The system of claim 4 wherein the alignment buffer includes a multitap delay element and a controller circuit, the multitap delay element having an input and a plurality of outputs and being configured to receive the STS-M signal at the input and provide increasingly delayed versions of the STS-M signal at successive ones of the outputs, the controller circuit being configured to select a delayed version of the STS-M signal from one of the outputs for application to the time slot interchange circuit.

6. The system of claim 1 wherein the at least one SONET input signal path comprises a plurality of SONET input signal paths and the at least one SONET output signal path comprises a plurality of SONET output signal paths,

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the number of SONET input signal paths being greater than the number of SONET output signal paths.

7. A SONET multiplexed communications system, comprising:

at least one SONET input signal path configured to receive at least one input signal;

at least one SONET output signal path configured to transmit at least one output signal corresponding to the input signal; and

at least one time slot interchange circuit operatively coupled between the SONET input and output signal paths and configured to provide time division multiplexed connections for the input and output signals,

wherein the SONET input signal path includes a synchronization buffer configured to transfer the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit, and

wherein the SONET output signal path includes a pointer interpreter configured to interpret at least one input signal pointer, a pointer generator configured to generate at least one output signal pointer, and a first-in first-out buffer serially coupled between the pointer interpreter and the pointer generator and configured to transfer the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path.

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8. The system of claim 7 wherein the input signal is an STS-M (M > 1) signal, and the SONET input signal path further includes an alignment buffer operatively coupled between the synchronization buffer and the time slot interchange circuit and configured to perform column alignment on the STS-M signal.

9. The system of claim 8 wherein the alignment buffer includes a multitap delay element and a controller circuit, the multitap delay element having an input and a plurality of outputs and being configured to receive the STS-M signal at the input and provide increasingly delayed versions of the STS-M signal at successive ones of the outputs, the controller circuit being configured to select a delayed version of the STS-M signal from one of the outputs for application to the time slot interchange circuit.

10. The system of claim 7 wherein the at least one SONET input signal path comprises a plurality of SONET input signal paths and the at least one SONET output signal path comprises a plurality of SONET output signal paths, the number of SONET input signal paths being greater than the number of SONET output signal paths.

11. A method of operating a SONET multiplexed communications system, comprising the steps of:

receiving at least one input signal by at least one SONET input signal path;

interpreting at least one input signal pointer by a pointer interpreter included in the SONET input signal path;

transferring the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of a time slot interchange circuit by a synchronization buffer included in the SONET input signal path;

providing time division multiplexed connections for the input signal and at least one corresponding output signal by the time slot interchange circuit;

generating at least one output signal pointer by a pointer generator included in at least one SONET output signal path;

transferring the corresponding output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path by a first-in first-out buffer included in the SONET output signal path; and

transmitting the corresponding output signal by the SONET output signal path.

12. The method of claim 11 further including the step of performing column alignment on the input signal by an alignment buffer included in the SONET input signal path.

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